Kenneth R. Allen, Reg. No. 27, 301 (650) 326-2400
Atty Docket No. 020510-10.00
Title: Flexible Buffering Scheme for Multi-Rate
SIMD Processor
Applicant: Fred Stacy, et al
Sheet 1 of 2

SINGLE
INSTRUCTION
DECODER

MULTIPLE DATAPATHS

12

PCU
PROGRAM
CONTROL
UNIT

DATA
RAM

DATA
RAM

13

14

14

PROGRAM
RAM

X

V

15

10

FIG. 1A
(PRIOR ART)

SINGLE
INSTRUCTION
DECODER

SINGLE DATAPATH—
TIME SHARED

12

PCU
PROGRAM
CONTROL
UNIT

DATA N–1

DATA 1
DATA 0

18

FOR EACH
INSTRUCTION

PROGRAM
RAM

DATA
RAM

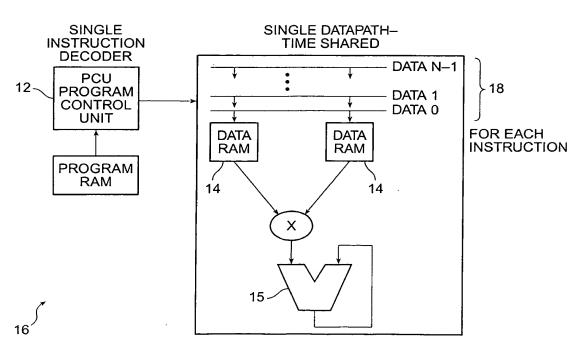DATA
RAM

14

14

X

V

15

16

FIG. 1B
(PRIOR ART)

Kenneth R. Allen, Reg. No. 27, 301 (650) 326-2400
Atty Docket No. 020510-1100
Title: Flexible Buffering Scheme for Multi-Rate
SIMD Processor
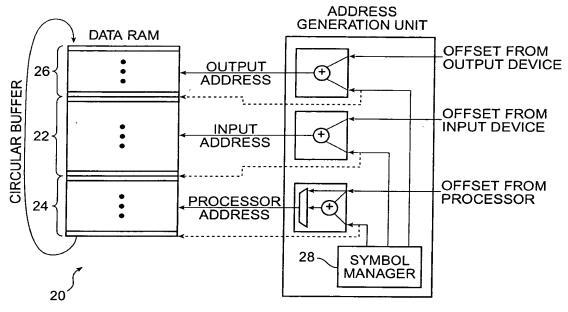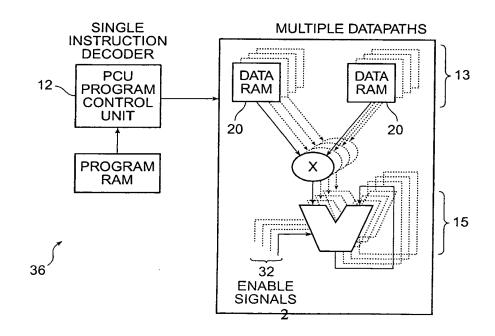Applicant: Fred Stacy, et al
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ADDRESS
GENERATION UNIT

DATA RAM

CIRCULAR BUFFER

26

OUTPUT
ADDRESS

OFFSET FROM
OUTPUT DEVICE

22

INPUT
ADDRESS

OFFSET FROM
INPUT DEVICE

24

PROCESSOR
ADDRESS

OFFSET FROM
PROCESSOR

28 — SYMBOL
MANAGER

20

FIG. 2

SINGLE
INSTRUCTION
DECODER

MULTIPLE DATAPATHS

12 — PCU
PROGRAM
CONTROL
UNIT

DATA
RAM

DATA
RAM

13

20

20

PROGRAM
RAM

X

15

32
ENABLE
SIGNALS

36

FIG. 3